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QUERY CONTROL FORM		RTIS USE ONLY	
Application No. <u>09925088</u>	Prepared by <u>JE</u>	Tracking Number <u>5909550</u>	
Examiner-GAU <u>Smith-2825</u>	Date <u>5-27-04</u>	Week Date <u>2-23-04</u>	
	No. of queries <u>1</u>	<u>IFW</u>	

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|----------------------|------------------------|--------------------|----------------|
| a. Serial No. | f. Foreign Priority | k. Print Claim(s) | p. PTO-1449 |
| b. Applicant(s) | g. Disclaimer | l. Print Fig. | q. PTOL-85b |
| c. Continuing Data | h. Microfiche Appendix | m. Searched Column | r. Abstract |
| d. PCT | i. Title | n. PTO-270/328 | s. Sheets/Figs |
| e. Domestic Priority | j. Claims Allowed | o. PTO-892 | t. Other |

SPECIFICATION

- a. Page Missing
- b. Text Continuity
- c. Holes through Data
- d. Other Missing Text
- e. Illegible Text
- f. Duplicate Text
- g. Brief Description
- h. Sequence Listing
- i. Appendix
- j. Amendments
- k. Other

CLAIMS

- a. Claim(s) Missing
- b. Improper Dependency
- c. Duplicate Numbers
- d. Incorrect Numbering
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- f. Punctuation
- g. Amendments
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- k. Other

MESSAGE

ON page 4 of 6 of the
 clm at the top there is
 a claim without a number
 followed by claim 21 (original
 claim 35).

THANK YOU
 JE

initials

RESPONSE

initials

(Previously Presented) The edge structure of claim 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are merged together.

²¹ 35. (Previously Presented) The edge structure of claim ¹² 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are not merged together.

²² 36. (Previously Presented) The edge structure of claim ¹² 25, wherein the first conductivity type is N type and the second conductivity type is P type.

²³ 37. (Previously Presented) The edge structure of claim ¹² 25, wherein the first conductivity type is P type and the second conductivity type is N type.

²⁴ 38. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion of the depletion region.

²⁵ 39. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions,

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